A GaAs HIGH-SPEED COUNTER USING CURRENT MODE LOGIC

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ABSTRACT

A single-clocked divide-by-four counter with maximum operating frequency of 3.4 GHz has been developed. The circuit was fabricated using a tungsten-silicide gate self-alignment technique with full ion implantation. The basic building block of the counter circuit is a current mode logic (CML) master-slave flip-flop similar to Si ECL.

INTRODUCTION

This paper will describe a high speed GaAs digital IC which is useful for microwave systems application. The circuit is based on the current mode logic (CML) gate which consists of a FET differential amplifier and a pair of buffer stages. The advantages of the circuit are that it can operate with single supply voltage and is fully compatible with Si ECL. In contrast, the disadvantage is that the FET differential amplifier usually exhibits lower voltage gain than bipoler transister one. To solve this problem, the self-alignment GaAs FET technique [1] is introduced. Two types of FETs with different threshold voltages and a ion implanted resistive layer are used to optimize the circuit performance.

DESIGN

The current-voltage characteristics of the GaAs FET are approximately written as

$$Id = K (Vgs - Vth)^2 \qquad (1)$$

where Id is the drain current, K is a constant, Vgs is the gate-source voltage and Vth is the threshold voltage of the FET. The transconductance is derived from (1) as

$$g_m = 2 K (Vgs - Vth) \qquad (2)$$

The K value which is determined experimentally is shown as a function of the threshold voltage in Fig. 1. This curve shows the distinct feature of the self-alignment GaAs FET, namely, the K value increases with the threshold voltage and is at it maximum in the positive threshold voltage (normally-off) region.

Fig. 2 shows the basic GaAs CML gate consisting of a differential amplifier and two source follower buffers with diode level shifters. If the input signal is applied to one of the driver FETs and the fixed reference voltage is applied to the other, the voltage gain at the balancing bias point will be given by

$$Gv = g_m RL/2 = \sqrt{KIo/2}\ RL = \sqrt{K/2Io}\ VL \qquad (3)$$

where RL is the load resistance, Io is the value of the current source and VL is the logic swing. Note that the voltage gain of this circuit is determined only by the load resistance, K value of the driver FETs and the drain current of the current source FETs. If the threshold voltage of the driver FETs are increased for increasing K value, the maximum drain current will be decreased. The driver FETs must flow the current of the current source FET. The maximum voltage applied to the gate is about 0.6 V, so that

$$I_{MAX} = K (0.6 - Vth)^2 > Io \qquad (4)$$

Higher threshold voltage (-0.4V) is utilized for the driver FETs to get higher voltage gain and smaller logic swing. Lower threshold voltage (-0.8V) is adapted for the current source FETs to suppress the deviation of drain current. Lower threshold voltage is also used for the buffer FETs to supply larger output current.

A CML master-slave flip-flop is designed using a clocked R-S flip-flop as shown in Fig. 3. A series gate configuration is utilized to achieve higher speed and lower power performance.

The schematic of the counter circuit is shown in Fig. 4. The asynchronous divide-by-four function is performed by two master-slave toggle flip-flops in series. The input is either capacitively coupled or DC coupled to the signal source. If the capacitive coupling is used, the input is biased in the middle of the transfer curve by an internal resistor connecting the clock input to the reference voltage. The two complementary open drain outputs are capable of driving 50-ohm lines and interfacing to ECL.

FABRICATION

The circuit chips were fabricated using a tungsten silicide gate self-alignment technique with multiple localized ion implantations. The key features of IC fabricating process are: (a) three selective implantations each optimized for load resistors, driver FETs, and buffer FETs, (b) sputtered tungsten-silicide gates, (c) high dosage implantation on both sides of the gates.

Fig. 5 shows a completed circuit. The chip measures 1 mm x 1 mm in size including the bonding pads, and contains 76 elements (high and low threshold voltage FETs and resistors). All the FETs except in the output stage, are 2 μm long and 40 μm wide. The FETs in the output stage are 400 μm wide and can handle the drain current greater than 20 mA. The level shift diodes are made of the low threshold voltage FETs by connecting the source and drain electrodes in parallel. The load resistors have the value of 1.2 Kohms.

PERFORMANCE

The IC chips were mounted in 14-lead flat packages for evaluation. Fig. 6 shows a block diagram of the test system used for microwave characterization. A microwave sweep oscillator supplies the clock input with sinewave signal. This signal is monitored through a return transmission line by a sampling oscilloscope. The two complementary open drain outputs of the counter are connected to the sampling oscilloscope and terminated by 50-ohm internal resistors.

Fig. 7 shows the microwave and low frequency operating waveforms of the counter. The maximum operating frequency was 3.4 GHz with the input amplitude of 1.3 V and the power dissipation of 240 mW at the supply voltage of -5 V. At 2 GHz, the input amplitude was lowered to 0.4 V with the same supply voltage. The circuits can drive external 50-ohm load with 1.3 V logic swing pulse and interface to ECL. For the low frequency measurement, the test setup of Fig. 6 was modified. A pulse generator is utilized as a signal source, clock and reference inputs are DC coupled and dual supply voltage (+2.5V and -2.5V) is applied.

The minimum amplitude of sinewave input for the correct operation is plotted as a function of frequency in Fig. 8. The input sensitivity was 0.2 V peak-to-peak at 1.8 GHz and reduced rapidly above 3 GHz. It reduced also below 1.5 GHz because of applying sinewave input. If the input signal with high slew rate is applied, it will operate at very low frequencies as demonstrated in Fig. 7(c). This circuit operates with single supply voltage. The operating range of the supply voltage is shown in Fig. 9. At 2 GHz, the counter correctly operates between -3 V and -6 V. The absolute maximum value of the supply voltage was ristricted to 6 V to prevent failure.

REFERENCE

[1] N. Yokoyama et al., "A GaAs 1K Static RAM Using Tungsten-Silicide Gate Self-Alignment Technology", in IEEE Int. Solid State Circuit Conf., Dig. Tech. Papers, Feb 1983, pp. 44-45.

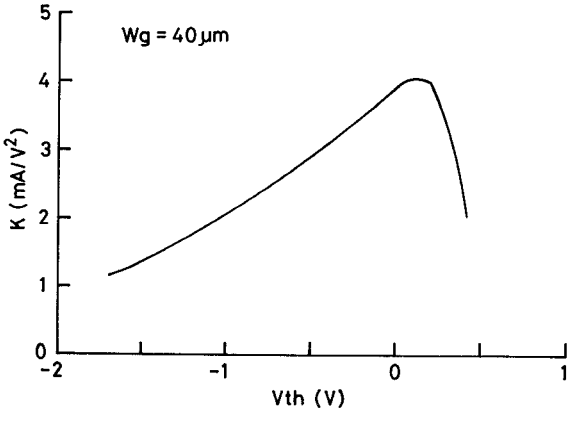


Fig. 1 K value and threshold voltage of the tungsten-silicide gate self-alignment GaAs FET. The gate length is 2 μm and width is 40 μm.

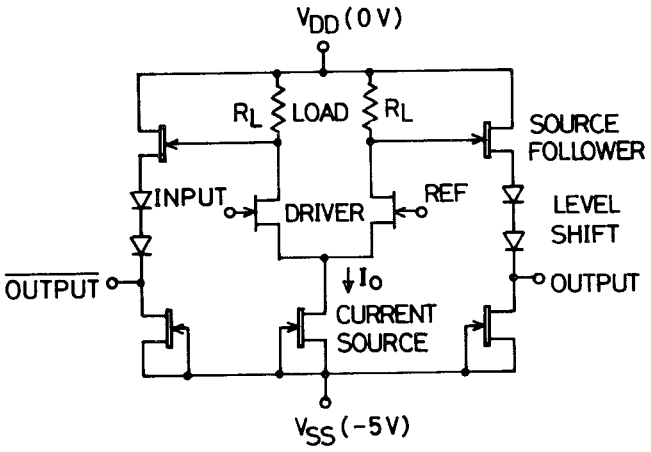


Fig. 2 Basic GaAs CML gate.

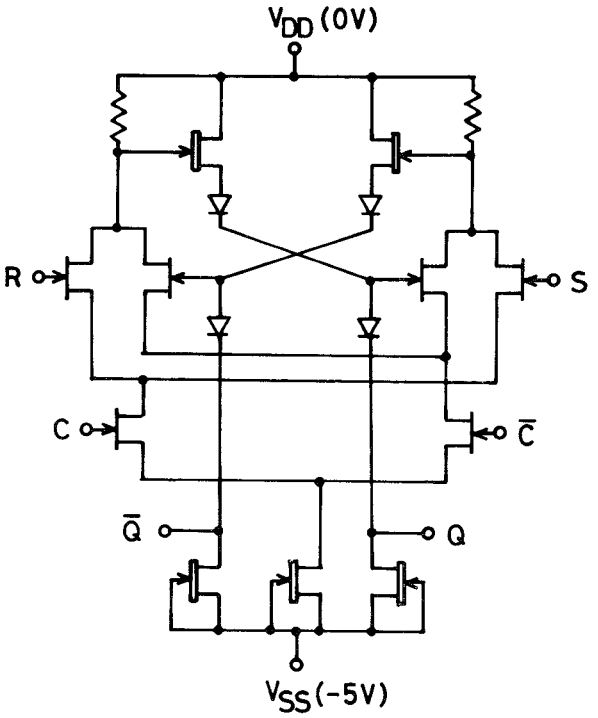


Fig. 3 Clocked R-S flip-flop with series gate configuration.

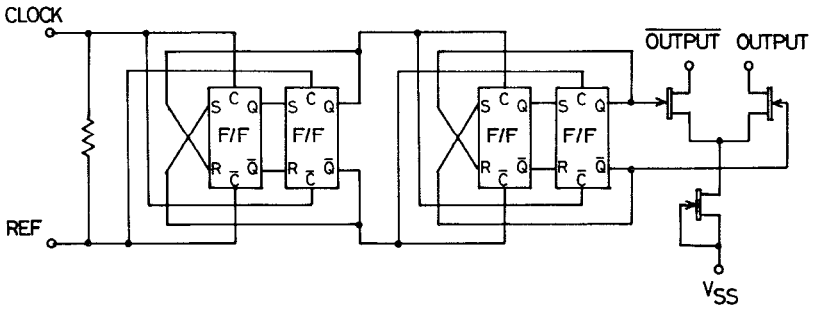


Fig. 4 Logic schematic of the divide-by-four counter.

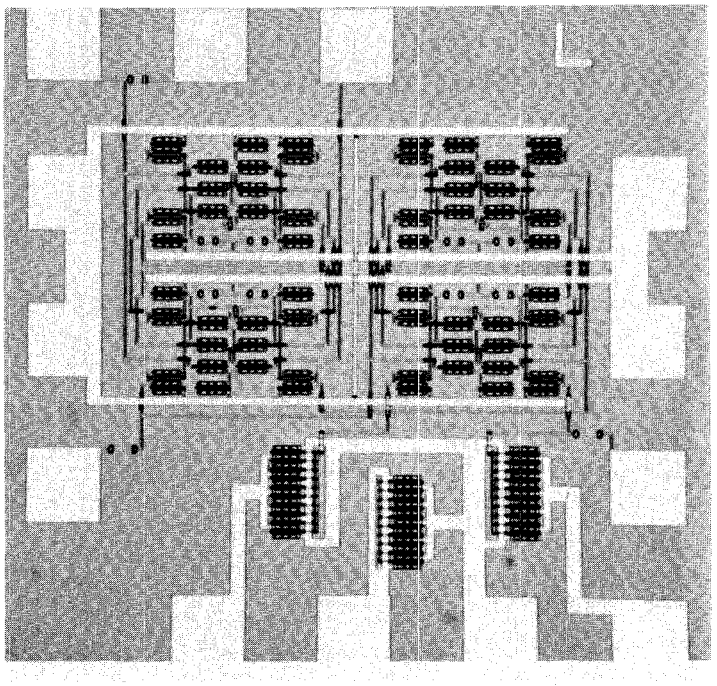
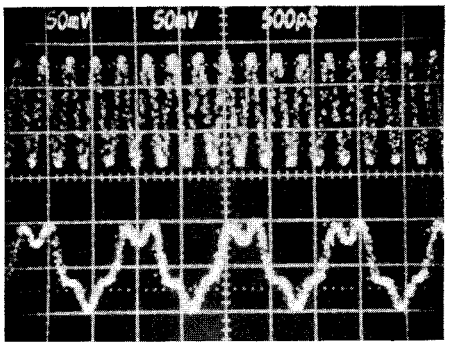
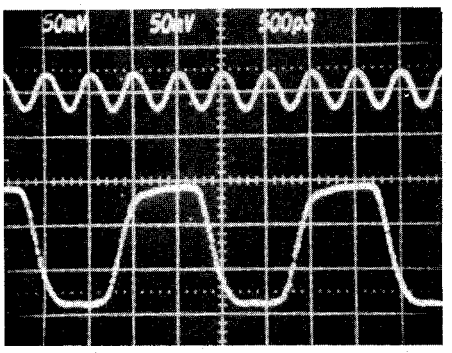


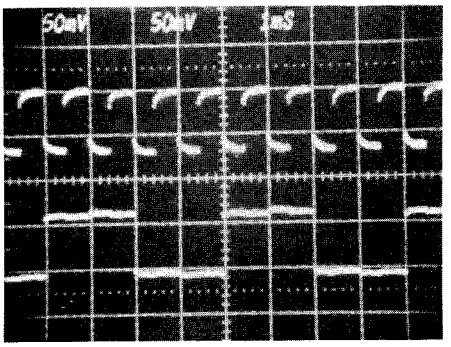
Fig. 5 Microphotograph of the counter chip. The chip size is 1 mm x 1 mm.



(a)



(b)



(c)

Fig. 7 Input and output waveforms of the counter at (a) 3.4 GHz, (b) 2 GHz and (c) 1 KHz.

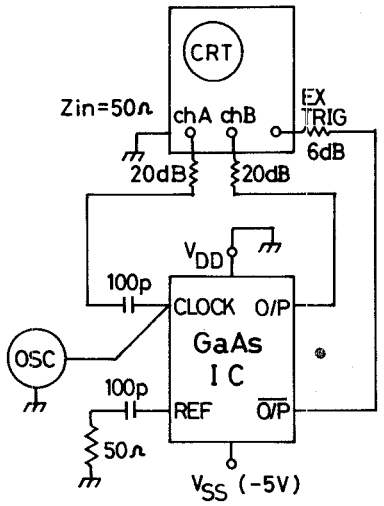


Fig. 6 Test setup for microwave circuit characterization.

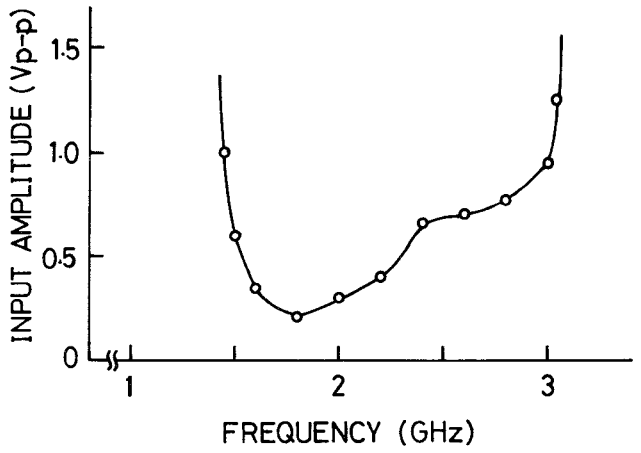


Fig. 8 Minimum amplitude of sinewave input as a function of frequency. The supply voltage is -5 V.

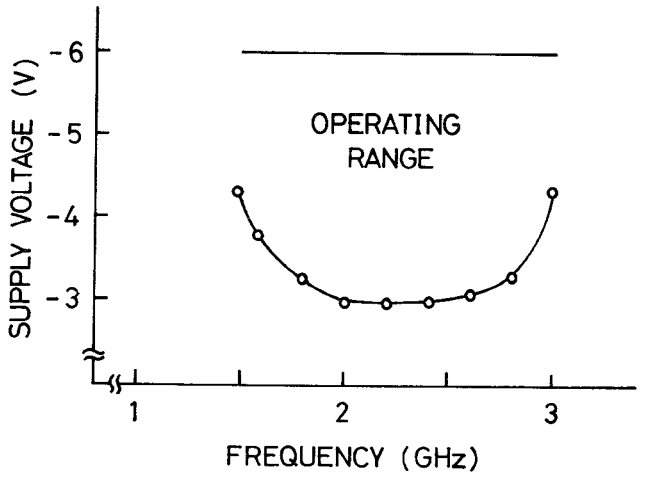


Fig. 9 Operating range of the supply voltage. The absolute value of the supply voltage was limited to 6 V.